REMARKS

In accordance with the foregoing, the claims have been amended to improve form and without change of substance.

Claims 1-20 are pending and under consideration.

ITEM 5: REJECTION OF CLAIMS 1-20 FOR OBVIOUNESS UNDER 35 U.S.C. §103 OVER FARRELL (U.S. PATENT 5,014,195) IN VIEW OF ALBONESI

It is noted that Farrell was supplied by applicant as Reference AA on IDS Form PTO-1449 whereas Albonesi was cited as Reference U on the Notice of References cited, Form PTO-892.

The rejections are respectfully traversed.

It is respectfully submitted that the Examiner has misinterpreted the references and the reliance on same as corresponding to the claimed invention herein.

(1) In general, tag/data memories as disclosed in Farrell do not have a concept of switching to a low consumption power mode.

Indeed, the Farrell reference employs no such terms therein such as "lower" or "higher", "power consumption" or any similar such terms, taken singularly or any relevant combination - - such as are employed by the Examiner in the Office Action rejections of the claims.

Indeed, despite purporting to read recitations of application claim 1 on Farrell, at page 3 of the Action, it is submitted that the readings are less than accurate. For example, both the "tag memory" and the "cache memory" are read on FIG. 2, respectively elements 34 and 42, and commonly at col. 4, lines 30-35. Nowhere in the text cited by the Examiner is there any reference to any elements being "capable of switching a state between an ordinary state and a lower power consumption state" as attributed to the cache memory section in claim 1. Indeed, as before noted, there is no reference anywhere in Farrell to power consumption or controlling/switching between ordinary and lower power consumption states.

Indeed, the Action further cites at page 3 "a control unit which controls [t]he switching of the way configuration..." which omits the significant term of:

a <u>power</u> control unit which controls switching of a way configuration....

In short, Farrell has no suggestion, much less any specific teaching, of a switching function relative to "a low consumption power mode" much less to switching between that state and "an ordinary state..." as recited in claim 1.

Furthermore, Farrell may be argued to have a disclosure of "a concept of switching between n-way set associative and 1-way set associative" - - but as follows from the foregoing, no such concept disclosed as a function of any "power control unit."

(2) In comparison to Farrell, Albonesi likewise is equally irrelevant in that "in general, tag/data memories do not have a concept of switching to a low consumption power mode."

Indeed, it again appears that the Examiner erroneously interprets Albonesi as disclosing a concept of switching to a low consumption power mode - - when, in fact, that does not appear in the disclosure and certainly has not been identified in any of the cited FIG. 1, Abstract or Sections 2 and 3.1 of Albonesi. (See page 4, first paragraph of the Office Action).

Unlike Farrell, Albonesi, moreover, fails to disclose any concept of "switching between n-way set associative and 1-way set associative" conditions.

Perhaps even more broadly, it does not appear that Albonesi discloses any concept of dynamically switching a physical state in response to a perameter - - and, indeed, there appears to be no disclosure in Albonesi of a circuit diagram or related function embodying a concept of dynamically switching a physical state using a parameter.

Accordingly, it is respectfully submitted that each of Farrell and Albonesi fails to teach or suggest that the respective cache memory units thereof are capable of switching a state between an ordinary state and a low consumption power state.

Clearly, as is apparent from claim 1 and as well from all other pending claims herein, the concept of switching between an ordinary state and a low consumption power state is at the crux of the present invention, as disclosed and claimed, and the same accordingly is submitted to distinguish patentably over the references, taken singularly or in any proper combination.

Indeed, the rejections are all the more deficient for failure to provide any *prima facie* demonstration of the alleged obviousness of combining the two references, under 35 MPEP 2143-2143.03.

CONCLUSION

In accordance with the foregoing, it is respectfully submitted that the foregoing has shown that the pending claims patentably distinguish over the references, taken singularly or in any proper combination and, further, there being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

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If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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